A Flip-Chip MMIC Design with Coplanar Waveguide Transmission Line in the W-Band

Tatsuya Hirose, Kozo Makiyama, Katsuji Ono, Tadayuki Miyata Shimura, Shigenori Aoki, Yoji Ohashi, Sigeru Yokokawa, and Yuu Watanabe, *Member, IEEE*

***Abstract*—This paper describes a design method for flip-chip monolithic millimeter-wave integrated circuits (MMIC's) with a coplanar waveguide (CPW) transmission line for W-band applications. We proposed a test structure for obtaining accurate flip-chip CPW line models. We examined the transmission line characteristics of the CPW line using the test structure in the millimeter-wave range and modeled them. Using the CPW line models, we designed and fabricated both two- and three-stage amplifiers using 0.15-μm InGaP/InGaAs high electron-mobility transistor technology. The maximum power gain of the two-stage amplifier is 12 dB at 79 GHz. The three-stage amplifier has a maximum power gain of 16 dB at 77 GHz. The agreement of measured S-parameters with calculated results demonstrates that the proposed test structure is suitable for characterizing flip-chip CPW lines and provides very accurate models.**

***Index Terms*—Amplifier, CPW, flip-chip, HEMT, W-band.**

I. Introduction

ALONG with the recent rapid increase in the demand for further improvements in automobile driving safety, systems are undergoing a transition from passive to active safety. Automotive radar systems working in the millimeter-wave range are one of candidates to provide the active safety, and interest is growing for the system's use in collision avoidance systems since it performs well in conditions of poor visibility. Several prototypes of W-band automotive radar systems based on the frequency-modulated continuous wave (FMCW) method, which consists of microstrip line (MSL) monolithic millimeter-wave integrated circuits (MMIC's), have been developed and the capability of their performance has been investigated [1]–[5].

These technologies are truly applicable to the development of millimeter-wave automotive radar systems. One of the most important issues in the utilization of millimeter-wave automotive radar systems is to reduce manufacturing costs. In general, manufacturing costs are still too high for installation of such radar systems into ordinary automobiles. This is primarily caused by the high costs involved in MMIC fabrication. In conventional MMIC fabrication that uses MSL technology, such complicated processes as wafer thinning, via hole etching, and backside processing of wafers have prevented decreases in manufacturing costs. In addition, the electrical performance of conventional wire bonding (WB) interconnections suffer from electrical discontinuities such as mismatch losses at the interconnections. The necessity for additional chip areas for matching circuits to compensate for those electrical discontinuities also contributes to the cost. For the following reasons, a combination of coplanar waveguide (CPW) transmission lines and flip-chip bonding technology (FCB) is one of the best ways to reduce the fabrication and assembly costs of MMIC's [6].

1) The wafer thinning process, via hole etching, and backside processing of the wafer is eliminated.
2) The electrical performance of shorter interconnection lengths is improved over wire bonding.
3) Fully automatic bonding is provided.

A great deal of research has been done on millimeter-wave applications based on FCB [6], [7]. An FCB technology using gold (Au) and gold–tin (AuSn) micropillars that are 20 μm tall and 40 μm in diameter has already been developed, and its excellent mechanical and thermal reliability for millimeter-wave applications has been reported [8]. In addition, the electrical performance of flipped CPW transmission lines have been thoroughly investigated, and the capability for millimeter-wave applications has been verified [9], [10]. Thus, the combination of CPW lines and FCB technology applied to the development and assembly of flip-chip MMIC's is very advantageous in achieving low-cost W-band automotive radar systems.

Despite the great advantages in combining CPW and FCB technology for manufacturing MMIC's, there is no accurate flip-chip CPW model for designing flip-chip MMIC's. This is because the signal transition parts such as pillars or bumps of an actual flip-chip CPW line are an electrical discontinuity that prevents the de-embedding of the external feed lines. The purpose of this paper is to present a technique to obtain an accurate flip-chip CPW model for designing W-band MMIC's that avoids the problems described above.

In the beginning of this paper, we pointed out the de-embedding problem at the signal transition pillar of the flip-chip CPW line using a three-dimensional (3-D) field simulator. We propose a test structure to characterize the flip-chip CPW lines accurately. The structure provides the same environment

Manuscript received March 30, 1998; revised September 2, 1998.

T. Hirose, K. Makiyama, K. Ono, T. M. Shimura, S. Aoki and Y. Watanabe are with Fujitsu Laboratories, Ltd., Atsugi-shi, Kanagawa 243–0197, Japan.

Y. Ohashi is with Fujitsu Laboratories, Ltd., Kawasaki-shi 211-8588, Kanagawa, Japan.

S. Yokokawa is with Fujitsu Quantum Devices, Ltd., Koufu-shi 409-3800, Yamanashi, Japan.

Publisher Item Identifier S 0018-9480(98)09207-2.

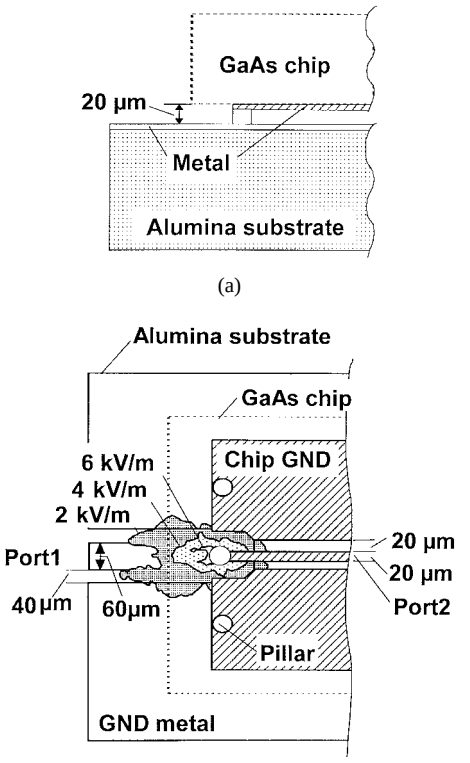


Fig. 1. Electromagnetic field simulation for an actual flip-chip CPW transmission line. (a) Side view of the analyzed structure. (b) Top view of the structure and calculated electromagnetic field distribution around signal transition pillar at 76 GHz.

with an actual flip-chip CPW line without a signal transition pillar. We applied the CPW line models with the test structure to the design and fabrication of W-band flip-chip MMIC two- and three-stage amplifiers using 0.15-μm InGaP/InGaAs high electron-mobility transistor (HEMT) technology. Through fabrication and evaluation, we demonstrate the validity of a flip-chip MMIC design with CPW transmission line.

II. Electromagnetic Field Analysis of Flip-Chip Structure

Fig. 1(a) and (b) show a portion of an analyzed flip-chip structure that includes a signal transition pillar. Fig. 1(a) is a side view of the structure. A 600-μm GaAs chip containing a CPW line is placed on a 200-μm-thick alumina ceramic substrate. A 2.0-μm-thick gold (Au) layer was coated on both the ground planes of the alumina ceramic substrate and the CPW line. The pillar height is 20 μm. Fig. 1(b) is a top view of the structure. The ground-to-ground spacing and the signal line width of the CPW line on the GaAs chip were 60 and 20 μm, respectively. For the CPW line on the alumina ceramic substrate, the ground-to-ground spacing and the signal line width were 140 and 60 μm, respectively. Here, the ground-to-ground spacing of the CPW line on the GaAs around the pillar was changed to minimize electrical discontinuity. Fig. 1(b) also shows the simulated results of a magnitude contour map of the time-averaged electric field distribution at a distance of 10 μm from the alumina ceramic substrate at 76 GHz. The simulation was performed using a three-dimensional full-wave electromagnetic field simulator (Ansoft Eminence). In this simulation, an electromagnetic wave was excited from port 1 with dominant mode excitation. As seen in Fig. 1(b), the electric field expands under the CPW line on the GaAs chip and the patterns are anomalous. This causes an interaction between the signal transition pillar and the CPW line.

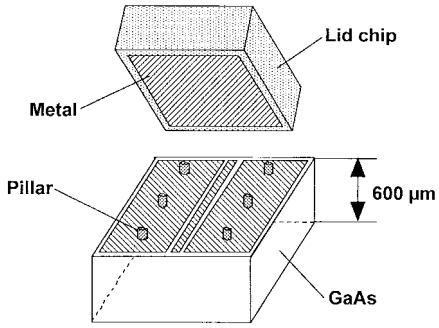


Fig. 2. Schematic diagram of the test structure. The metal surface of the lid chip faces the CPW line.

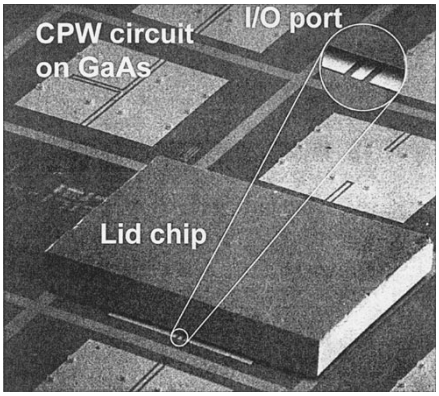
Generally, de-embedding can be used for lines if the geometry along the line is maintained. If the de-embedding process is used for lines that have discontinuities or a tapered line, physically incorrect results will occur. Correct results require a homogeneous electromagnetic field distribution along the line. Therefore, it is difficult to determine the reference plane for de-embedding lines that include signal transition pillars.

In order to characterize flip-chip CPW lines accurately, we propose a test structure that provides the same environment as an actual flip-chip CPW line without signal transition pillars.

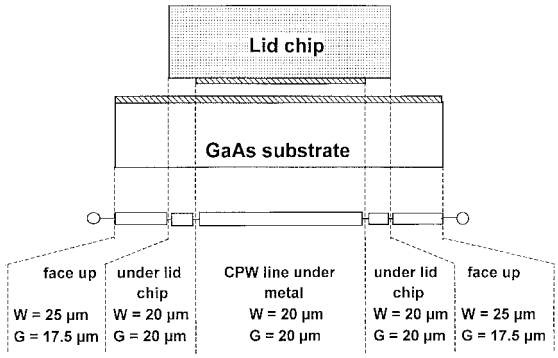
III. The Test Structure

The test structure consists of two parts. One part is a CPW line fabricated on a 600-μm thick GaAs substrate. Here, 2.0-μm-thick gold (Au) is used for the CPW line. The other part is a lid chip whose entire surface is coated with Au. This chip is used as a ground lid of the CPW line and is positioned above it (Fig. 2). The lid chip is mounted by a flip-chip bonding tool that guarantees precise positioning on micropillars fabricated on the CPW line's ground so that the metallized surface faces the CPW line [8]. The pillar height, diameter, and the minimum distance between pillars are 20, 40, and 125 μm, respectively. Although this test structure differs from the actual flip-chip structure, the electrical characteristics of the CPW lines are almost the same because a sufficiently thick GaAs substrate is employed, meaning that there is no surface leakage [10]. Fig. 3(a) and (b) shows the structure and corresponding CPW line. As seen in Fig. 3(b), there are three parts for the CPW line structure: the face-up feed line, the line that lies underneath the lid chip, and the line under the metal. The line width was tuned to minimize electrical discontinuity at the interface between the face-up part and the ground-face part. The most important feature of this structure is to be able to measure the electrical performances of the flip-chip CPW line without signal transition pillars. In addition, as seen in Fig. 3(a), this structure enables on-wafer measurements.

To characterize the transmission line characteristics of the CPW line using the test structure, we measured the



(a)



(b)

Fig. 3. Test structure. (a) SEM micrograph. (b) CPW lines corresponding to the test structure.

S-parameters using a vector network analyzer (VNA) with coplanar ground–signal–ground microprobes in the frequency range of 0.45–110 GHz. The transmission line parameters were extracted from the measured S-parameters. Fig. 4 is a plot of the extracted and calculated transmission line parameters of the CPW through-line after de-embedding the feed lines and the lines beneath the lid chip. The calculation was performed with the moment method using the Gelerkin technique [11]. In the W-band, the attenuation constant in the propagation constant of the actual transmission lines expression $(Z = \sqrt{(R+j\omega L)/(G+j\omega C)})$ can be smaller than the phase constant, i.e., $RG \ll \omega^2 LC$. Therefore, we used the following equations (see the Appendix):

$$Z_0 = \sqrt{\frac{L}{C}} \quad (\Omega) \tag{1}$$

$$E_{\text{eff}} = L \cdot C \cdot c_0^2 \tag{2}$$

$$A_{ttn} = \frac{R}{2 \cdot Zo \cdot 0.115\,129} \cdot \sqrt{\frac{F_C}{f_0}} \quad \text{dB/m} \tag{3}$$

$$\tan\delta = \frac{G}{2\pi \cdot f_0 \cdot C} \tag{4}$$

where Z_0 is the lossless characteristic impedance, E_{eff} is the effective dielectric constant, A_{ttn} is the conductor loss of the line, and $\tan\delta$ is a dielectric loss tangent. L, C, R, and G are the inductance, capacitance, resistance, and conductance per unit length of the transmission line, respectively. F_C is a reference frequency where the conductor attenuation is dominant. f_0 is a simulation frequency, and c_0 is the velocity of light. De-embedding was carried out with an ABCD matrix manipulation. From the measured data for the line width of 20 μm, a ground-to-ground spacing of 60 μm, and a pillar height of 20 μm, we obtained $Z_0 = 49.0\ \Omega$, $E_{\text{eff}} = 5.41$, $A_{ttn} = 300$ dB/m and $\tan\delta = 1.4 \times 10^{-3}$. For a line without the lid chip, we also obtained $Z_0 = 55.9\ \Omega$, $E_{\text{eff}} = 6.33$, $A_{ttn} = 241$ dB/m, and $\tan\delta = 1.6 \times 10^{-3}$ with the same line width and ground-to ground spacing. An interaction between the CPW line and ground on the substrate was observed [9], [10]. These results closely agree with the simulation results and indicate that W-band flip-chip MMIC's that use a CPW line can be designed using a quasi-TEM mode approximation. Using the test structure, we measured various types of CPW lines such as T-junctions, cross junctions, bends, and so on, and extracted the transmission line parameters. We also added the model to the HP-EEsof Libra circuit simulator.

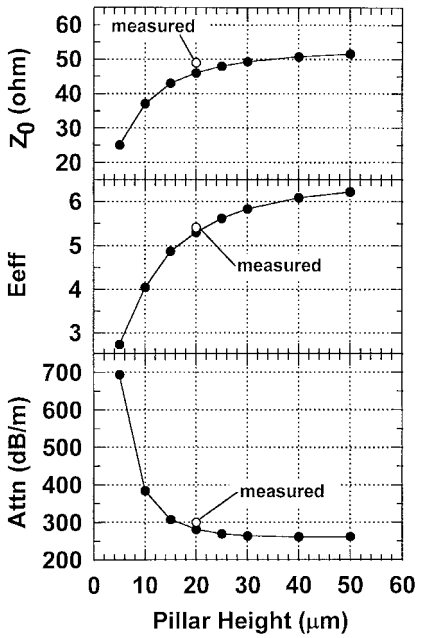


Fig. 4. Simulated and extracted transmission line parameters of the CPW line using the test structure. The line width and gaps are 20 μm, respectively.

IV. Design and Fabrication of Flip-Chip MMIC's

A. 0.15-μm InGaP/InGaAs HEMT Technology

To verify the accuracy of the CPW line model with the test structure, we designed and fabricated two- and three-stage amplifiers for the W-band. For the circuit design, we employed an InGaP/InGaAs HEMT on a semi-insulated GaAs substrate with a 0.15-μm-long mushroom-shaped gate electrode drawn by electron-beam lithography (EB). Epitaxial layers were grown with metal-organic vapor-phase-epitaxial growth (MOVPE). A schematic cross section of the InGaP/InGaAs HEMT is shown in Fig. 5. Fig. 6 plots the small-signal frequency characteristics of an 80-μm-wide HEMT with a bias condition of $V_{DS} = 3$ V and $V_{GS} = -0.4$ V. It shows a cutoff frequency (f_T) of 90 GHz, a maximum oscillation frequency $(f_{\max})$ of 170 GHz, and a maximum stable gain (MSG)

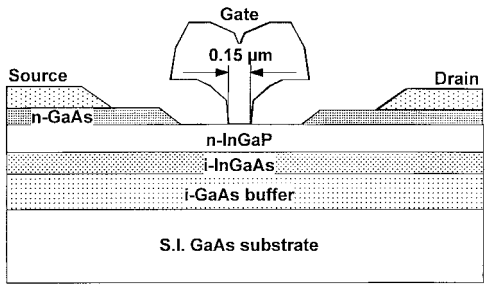


Fig. 5. Schematic cross section of a 0.15-μm InGaP/InGaAs HEMT.

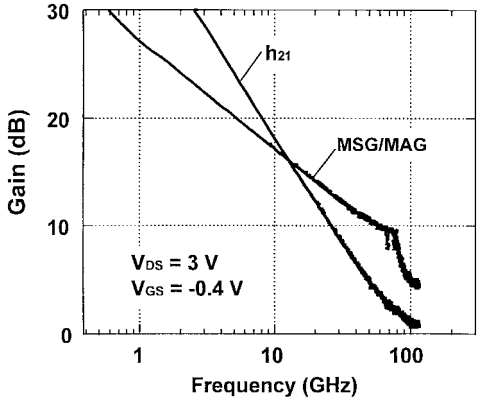


Fig. 6. Frequency characteristics of a 0.15-μm InGaP/InGaAs HEMT. The gate width is 80 μm.

of 9 dB at 76 GHz. Here, $f_{\max}$ was determined from the maximum available gain characteristics instead of the -6-dB extrapolation of the unilateral power gain characteristics. We also measured the RF characteristics of an 80-μm-wide HEMT with the test structure having a pillar height of 20 μm and CPW lines. Several of the parameters exhibited small changes, but these deviations are almost negligible for the MMIC design. The source inductance also did not change. The result indicates that face-up HEMT equivalent circuit parameters can be used in MMIC design.

B. Flip-Chip-Mounted MMIC Structure

To examine the performance of a flip-chip-mounted MMIC, we used an alumina ceramic substrate with patterned dc and RF feed lines on its surface. Fig. 7 is an SEM micrograph of the flip-chip-mounted MMIC. Several capacitor subchips were also mounted to eliminate unexpected oscillation in the low-frequency range. The substrate size was 8 mm $\times$ 8 mm. All MMIC's had Au pillars 20 μm tall and 40 μm in diameter. Flip-chip bonding was performed with a pulse-heated bonding tool, which guaranteed accurate positioning [8].

C. Two- and Three-Stage Amplifiers

For design of the two-stage and three-stage amplifier, we employed an 80-μm-wide gate HEMT. The design was based on the small-signal design. As mentioned above, since the small-signal equivalent circuit parameters of the HEMT under the test structure were the same as the face-up one, we used face-up data for the design. The measurements of the HEMT

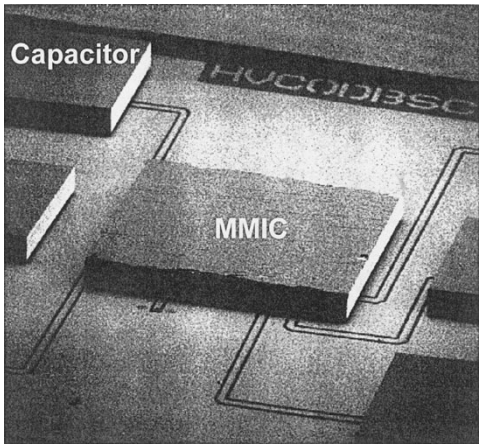


Fig. 7. SEM micrograph of the flip-chip-mounted MMIC.

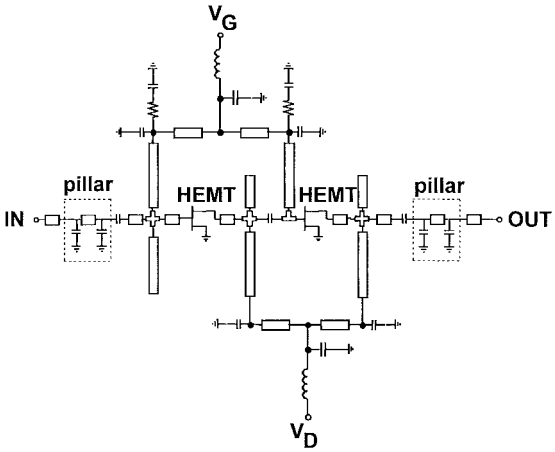


Fig. 8. Schematic diagram of a two-stage amplifier.

small-signal S-parameters were on-wafer measurements. Open circuited stubs were used for the input, output, and inter-stage matching circuits. The characteristic impedance and effective dielectric constant of the signal transition pillars were estimated via a 3-D electromagnetic field simulator [14]. The estimated characteristic impedance of the pillar was 207 Ω, and the dielectric constant was 1. Schematic diagrams of the equivalent circuit for the two- and three-stage amplifiers are shown in Figs. 8 and 9. In this case, the effect of the additional signal transition pillar model on the total characteristics of the MMIC performance was negligible [9]. Fig. 10 is a micrograph of the two-stage MMIC amplifier chip. The chip size was 1.9 mm $\times$ 1.25 mm. Fig. 11 is a micrograph of the three-stage MMIC amplifier chip whose size is 1.9 mm $\times$ 2.5 mm.

The amplifier was tested using a VNA from 75 to 110 GHz. Fig. 12 plots the measured S-parameters of the biased flip-chip two-stage amplifier with $V_D = 3$ V and $V_G = -0.6$ V. The forward gain (S_{21}) and isolation (S_{12}) at 79 GHz were 12 and -27 dB, respectively. The input (S_{11}) and output return losses (S_{22}) were -20 and -10 dB, respectively. Fig. 13 shows the measured S-parameters of the three-stage amplifier with a $V_D = 3$ V and $V_G = -0.4$ V for the gate. The obtained forward gain at 77 GHz (S_{21}) and isolation (S_{12}) were 16

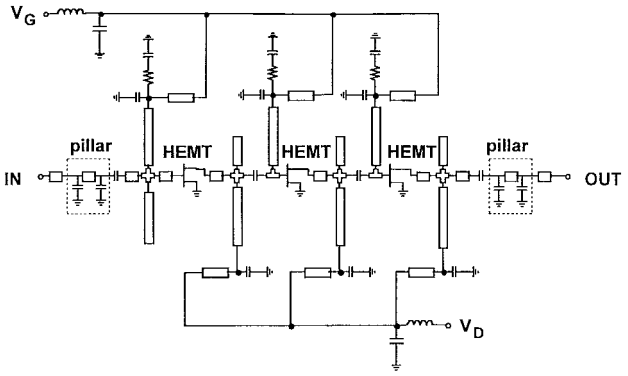


Fig. 9. Schematic diagram of a three-stage amplifier.

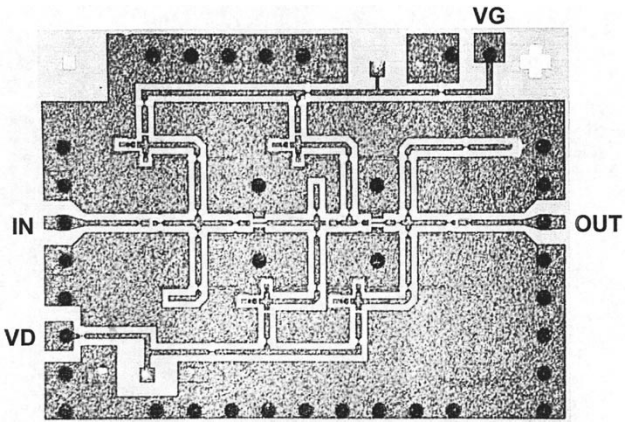


Fig. 10. Two-stage amplifier. The chip size is 1.9 mm × 1.25 mm.

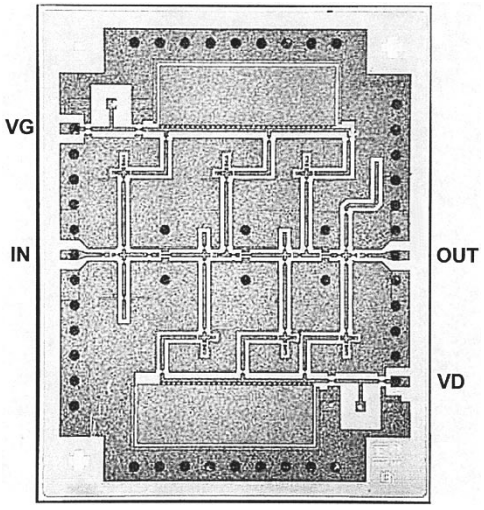


Fig. 11. Three-stage amplifier. The chip size is 1.9 mm × 2.5 mm.

and −34 dB, respectively. The input (S_{11}) and output return losses (S_{22}) were −11 and −2 dB, respectively. The measured data closely matches the simulated results.

V. Conclusion

Through an analysis of electromagnetic field distribution around the signal transition pillars of a flip-chip CPW structure by means of a 3-D electromagnetic field simulation, we have shown the difficulties of the de-embedding process in modeling flip-chip CPW transmission lines. We proposed a test structure to model flip-chip CPW transmission lines in order to design flip-chip-mounted MMIC's for W-band automotive radar systems. The test structure provides the same environment of an actual flip-chip CPW line without the signal transition pillar. We applied the model to the design of 0.15-μm InGaP/InGaAs HEMT flip-chip-mounted MMIC two- and three-stage amplifiers. We obtained maximum power gains of 12 dB at 79 GHz for the two-stage amplifier and 16 dB at 77 GHz for the three-stage amplifier. These amplifiers exhibit sufficient performance for commercial applications of 76 GHz automotive radar systems. In addition, the level of agreement between the calculated S-parameters and the measured data suggests that the flip-chip CPW line modeling technique demonstrated here is valid for designing flip-chip MMIC's.

This flip-chip CPW modeling technique is essential for developing low-cost flip-chip MMIC's for W-band applications as well as for millimeter-wave automotive radar systems.

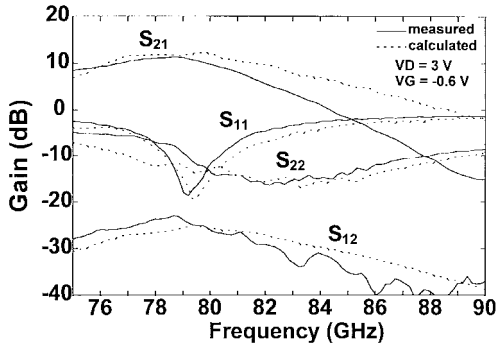


Fig. 12. Measured and calculated S-parameters of the flip-chip InGaP/InGaAs HEMT MMIC two-stage amplifier.

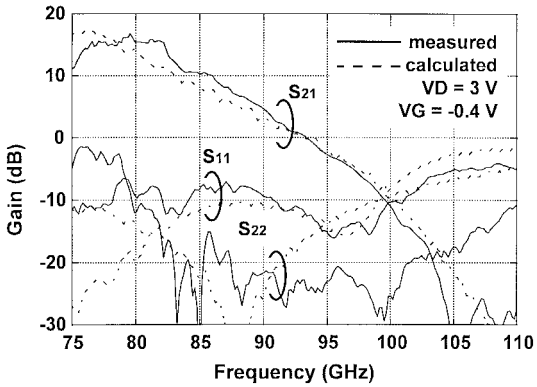


Fig. 13. Measured and calculated S-parameters of the flip-chip InGaP/InGaAs HEMT MMIC three-stage amplifier.

Appendix

To derive (3), assuming that $RG \ll \omega^2 LC$ for low-loss lines, a propagation constant of an actual transmission line

was given by [12]

$$\gamma = \alpha + j\beta = \sqrt{(RB - \omega^2 LC) + j\omega(LG + RC)}$$

$$\approx j\omega\sqrt{LC \cdot \left[1 + \frac{j\omega(LG+RC)}{-\omega^2 LC}\right]}. \quad \text{(A1)}$$

Using the binomial expansion theorem

$$(1+x)^{1/2} \approx 1 + \frac{1}{2}x - \frac{1}{8}x^2 + \cdots \quad \text{(A2)}$$

gives

$$\alpha + j\beta \approx j\omega\sqrt{LC} + \frac{LG+RC}{2\sqrt{LC}}. \quad \text{(A3)}$$

In (A3), the attenuation constant α can be separated by conductor loss part α_c and dielectric loss part α_d. The value of α_c is expressed as follows:

$$\alpha_c = \frac{R}{2}\sqrt{\frac{C}{L}} = \frac{R}{2Z_0} = \frac{\sqrt{\pi\mu\rho}}{Z_0 \cdot W}\sqrt{f_0} \quad \text{(A4)}$$

where f_0 is frequency, W is the transmission line width, μ is permeability, and ρ is the resistivity of the conductor. Here, the conductor loss at frequency F_c is given by

$$A_{ttn} = \frac{\sqrt{\pi\mu\rho}}{Z_0 \cdot W}\sqrt{F_c}. \quad \text{(A5)}$$

Substituting (A5) into (A4), we obtain the following expressions for A_{ttn} in decibels per unit length:

$$A_{ttn} = \frac{R}{2 \cdot Z_0 \cdot 0.115129} \cdot \sqrt{\frac{F_c}{f_0}} \quad \text{dB/m}. \quad \text{(A6)}$$

ACKNOWLEDGMENT

The authors would like to thank M. Takikawa, N. Okubo, and T. Yokoyama for their encouragement. They also thank M. Nishi and H. Someta for fabricating the test structure, and T. Shimura for his helpful discussions on MMIC design.

REFERENCES

[1] M. Berg, J. Dickmann, R. Guehl, and W. Bischof, "60–77 GHz monolithic amplifiers utilizing InP-based HEMT's and coplanar waveguides," *Microwave Optical Technol. Lett.*, vol. 11, no. 3, pp. 139–145, Feb. 1996.

[2] W. H. Haydl, L. Verweyen, T. Jakobus, M. Newumann, A. Tessmann, T. Krems, M. Schlechtweg, W. Rinert, H. Massler, J. Rudiger, W. Bronner, A. Hulsmann, and T. Fink, "Compact monolithic coplanar 94 GHz front ends," in *IEEE MTT-S Dig.*, 1997, pp. 1281–1284.

[3] J.-E. Muller, T. Grave, H. J. Siweris, M. Kārner, A. Schäfer, H. Tischer, H. Riechert, L. Schleicher, L. Verweyen, A. Bangert, W. Kellner, and T. Meier, "A GaAs HEMT MMIC chip set for automotive radar systems fabricated by optical stepper lithography," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1342–1348, Sept. 1997.

[4] M. E. Russell, A. Crain, A. Curran, R. A. Campbell, C. A. Drubin, and W. F. Miccioli, "Millimeter-wave radar sensor for automotive intelligent cruise control (ICC)," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2444–2453, Dec. 1997.

[5] K. Kamozaki, N. Kurita, W. Hioe, T. Tanimoto, H. Ohta, T. Nakamura, and H. Kondoh, "A 77 GHz T/R MMIC chip set for automotive radar systems," in *19th Annu. IEEE GaAs IC Symp. Dig.*, Anaheim, CA, Oct. 1997, pp. 275–278.

[6] G. Baumann, D. Ferling, and H. Richter, "Comparison of flip chip and wire bond interconnections and the technology evaluation on 51 GHz transceiver modules," in *26th Eur. Microwave Conf. Proc.*, 1996, pp. 98–100.

[7] H. Sakai, Y. Ota, K. Inoue, T. Yoshida, K. Takahashi, S. Fujita, and M. Sagawa, "A novel millimeter-wave IC on Si substrate using flip-chip bonding technology," in *IEEE MTT-S Dig.*, 1994, pp. 1763–1766.

[8] S. Aoki, H. Someta, S. Yokokawa, K. Ono, T. Hirose, and Y. Ohashi, "A flip chip bonding technology using gold pillars for millimeter-wave applications," in *IEEE MTT-S Dig.*, 1997, pp. 731–734.

[9] T. Krems, W. Haydl, H. Massler, and J. Rudiger, "Millimeter-wave performance of chip interconnections using wire bonding and flip chip," in *IEEE MTT-S Dig.*, 1996, pp. 247–250.

[10] T. Krems, W. Haydl, H. Massler, and J. Rudiger, "Advantages of flip chip technology in millimeter-wave packaging," in *IEEE MTT-S Dig.*, 1997, pp. 987–990.

[11] M. B. Bazdar, A. R. Djordjevic, R. F. Harrington, and T. K. Sarkar, "Evaluation of quasistatic matrix parameters for multiconductor transmission lines using Galerkin's method," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1223–1228, July 1994.

[12] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. New York: Wiley, 1990.

[13] R. Sturdivant, "Reducing the effects of the mounting substrate on the performance of GaAs MMIC flip chips," in *IEEE MTT-S Dig.*, 1995, pp. 1591–1594.

[14] Y. Arai, M. Sato, H. T. Yamada, T. Hamada, K. Nagai, and H. I. Fujishiro, "60 GHz flip-chip assembled MIC design considering chip-substrate effect," in *IEEE MTT-S Dig.*, 1997, pp. 447–450.

Tatsuya Hirose received the B.E. degree from Tokyo Denki University, Tokyo, Japan, in 1987 and the M.E. degree from Hokkaido University, Sapporo, Japan, in 1989.

In 1989, he joined Fujitsu Laboratories, Ltd., Atsugi, Japan, where he has been engaged in research on characterization and modeling for heterostructure devices and the development of MMIC's based on their technologies. His current research interest includes microwave and millimeter-wave integrated circuit design for automotive radar systems and wireless communication systems.

Mr. Hirose is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan.

Kozo Makiyama received the B.E. and M.E. degrees from the Osaka Institute of Technology, Osaka, Japan, in 1986 and 1988, respectively.

In 1988, he joined Fujitsu Laboratories, Ltd., Atsugi, Japan, where he has been engaged in research and development of HEMT device technologies.

Mr. Makiyama is a member of the Japan Society of Applied Physics.

Katsuji Ono received the B.E. and M.E. degrees from the University of Electro-Communications, Tokyo, Japan, in 1985 and 1987, respectively.

In 1987, he joined Fujitsu Laboratories, Ltd., Atsugi, Japan, where he has been engaged in research and development of high-speed HEMT integrated circuits.

Mr. Ono is a member of the Japan Society of Applied Physics.

Tadayuki Miyata Shimura received the B.E. and M.E. degrees from Shizuoka University, Shizuoka, Japan, in 1988 and 1990, respectively.

In 1990, he joined Fujitsu Laboratories, Ltd., Atsugi, Japan, where he has been engaged in the research and development of HEMT LSI's and MMIC's.

Mr. Shimura is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan.

Shigenori Aoki received the B.S. degree from Kyoto University, Kyoto, Japan, in 1985.

In 1985, he joined Fujitsu Laboratories, Ltd., Atsugi, Japan, where he has been engaged in the research and development of packaging technology for microconnection and ceramic substrate.

Mr. Aoki is a member of the Japan Institute of Electronics Packaging.

Yoji Ohashi received the B.S. degree in physics and M.S. degree in astrophysics from Nagoya University, Nagoya, Japan, in 1984 and 1986, respectively.

He joined Fujitsu Laboratories, Ltd., Kanagawa, Japan, in April 1986. He has developed cryogenically cooled low-noise amplifiers for radio astronomy since 1991. He has studied noise equivalent circuits of HEMT's. His present research activities are connected with millimeter-wave HEMT monolithic integrated circuit design.

Sigeru Yokokawa graduated from Isikawa Technical High School, Isikawa, Japan, in 1968.

From 1968 to 1985, he worked in the Compound Semiconductor Laboratory of Fujitsu Laboratories, Ltd., where he has been engaged in research and development of process technologies for Gunn diode and GaAs MMIC's. In 1985, he moved to Fujitsu Ltd., where he was engaged in development of GaAs LSI's. In 1997, he joined the Fujitsu Quantum Devices Ltd., Yamanashi, Japan. His current interests are millimeter-wave MMIC's and their applications.

Yuu Watanabe (M'87) was born in Fukuoka, Japan, in 1956. He received the B.S. and M.E. degrees from Kyoto University, Kyoto, Japan, in 1980 and 1982, respectively, and the Ph.D. degree from Osaka University, Osaka, Japan, in 1997.

In 1982 he joined Fujitsu Laboratories, Ltd., Kanagawa, Japan, where he has been engaged in the research and development of heterostructure devices. His current research includes HEMT's, HBT's, tunneling devices, and their circuits.

Dr. Watanabe served as Secretary of the VLSI Circuit Symposium in 1990 and 1991. He is a member of Institute of Electronics, Information, and Communication Engineers (IEICE), Japan.